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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/076,355	02/19/2002	Tomio Yamashita	020167	1518

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EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/076,355	YAMASHITA, TOMIO	
	Examiner	Art Unit	
	Hung K. Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-14* is/are pending in the application.

4a) Of the above claim(s) *5 and 11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,6-10 and 12-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1 A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant' submission filed on 10/29/03 has been entered. An action on the RCE follows.

Claim Objections

2. Claims 4, 6-10 and 12 are objected to because of the following informalities:

In claim 4, lines 1-2, "the conductive" should be changed to "the upper conductive" for clarity.

In claim 6, lines 5 and 6, after "one" insert --first-- for clarity.

In claim 6, lines 11 and 13, after "one" insert --second-- for clarity.

In claim 6, line 12, "a conductive portion" should be changed to "an upper conductive portion" for clarity.

In claim 6, last two lines, "the upper dielectric layer and the lower dielectric layer" should be changed to "the upper conductive portion and the lower conductive portion" for clarity.

In claim 7, line 2, "the dielectric film" should be changed to "the lower dielectric layer" for clarity.

In claim 8, lines 2 and 3, "the dielectric film" should be changed to "the lower dielectric layer" for clarity.

In claim 9, line 2, after "one" insert --first-- for clarity.

In claim 10, line 2, "the dielectric film" should be changed to "the lower dielectric layer" for clarity.

In claim 12, line 5, after "one" insert --first-- for clarity.

In claim 12, line 6, "the conductive metal" should be changed to "the lower conductive metal" for clarity.

In claim 12, line 11, after "one" insert --second-- for clarity.

In claim 12, line 12, "the conductive metal" should be changed to "the upper conductive metal" for clarity.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4, 6-10 and 12-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka (PN 6,100,589).

Tanaka discloses, as shown in Figures 1, 7A, 7B, and 22, a semiconductor device having a multilayer wiring structure, comprising:

a semiconductor substrate (400);

a lower dielectric layer (lower portion 160) arranged on the substrate and having an opening, a conductive portion (300) filling the opening, and at least one dielectric member (133a-133i) embedded in the conductive portion;

an interlayer dielectric film (upper portion 160) arranged on the lower dielectric layer and having a contact wiring (120a-120c);

an upper dielectric layer (lower portion 150) arranged on the interlayer dielectric film and having an upper opening, an upper conductive portion (200) filling the upper opening, and at least one dielectric member (130a-130i) embedded in the upper conductive portion, wherein the upper dielectric layer and the lower dielectric layer are electrically connected by the contact wiring.

With regard to claim 2, Tanaka discloses at least one dielectric member is arranged in an island-like manner in the opening.

With regard to claim 4, Tanaka discloses the upper conductive portion includes an external electrode terminal (180).

With regard to claim 6, Tanaka discloses, as shown in Figures 1, 7A, 7B, and 22, a semiconductor device having a multilayer wiring structure, comprising:

a semiconductor substrate (400);

a lower dielectric layer (lower portion 160) arranged on the substrate and including an upper surface, a lower surface, an opening, at least one first dielectric member arranged in the opening (133a-133i), and a conductive portion (300) filling the opening so as to surround the at least one first dielectric member;

an interlayer dielectric film (upper portion 160) arranged on the lower dielectric layer and having a contact wiring (120a-120c);

an upper dielectric layer (lower portion 150) arranged on the interlayer dielectric film and having an upper opening, at least one second dielectric member (130a-130i) arranged in the upper opening, and an upper conductive portion (200) filling the upper opening so as to surround the at least one second dielectric member, wherein the upper conductive portion and the lower conductive portion are electrically connected by the contact wiring.

With regard to claim 7, Tanaka discloses the at least one first dielectric member has a height that is the same as the thickness of the lower dielectric layer.

With regard to claim 8, Tanaka discloses the at least one first dielectric member has an end flush with the upper surface of the lower dielectric layer and a further end flush with the lower surface of the lower dielectric layer.

With regard to claim 9, Tanaka discloses the at least one first dielectric member is one of a plurality of separated dielectric members.

With regard to claim 10, Tanaka discloses the conductive portion has a flat surface flush with the upper surface of the lower dielectric layer.

With regard to claim 12, Tanaka discloses, as shown in Figures 1, 7A, 7B, and 22, a semiconductor device comprising:

a semiconductor substrate (400);

a lower dielectric layer (lower portion 160) arranged on the semiconductor substrate and having a lower pad, wherein the lower pad includes a lower through hole, a lower conductive metal (300) filling the lower through hole, and at least one first dielectric member (133a-133i) enclosed by the lower conductive metal;

an interlayer dielectric film (upper portion 160) arranged on the lower dielectric layer and having a contact wiring (120a-120c);

an upper dielectric layer (lower portion 150) arranged on the interlayer dielectric film having an upper pad, wherein the upper pad includes an upper through hole, an upper conductive metal (200) filling the upper through hole, and at least one second dielectric member (130a-130i) enclosed by the upper conductive metal, and therein the upper conductive metal is electrically connected to the lower conductive metal via the contact wiring of the interlayer dielectric film.

With regard to claim 13, Tanaka discloses the lower conductive portion and the upper conductive portion are arranged vertically.

With regard to claim 14, Tanaka discloses the contact wiring of the interlayer dielectric film includes a through hole, a conductive metal filling the through hole, and at least one dielectric member enclosed by the conductive metal [Col. 8, line 39-41].

Response to Arguments

4. Applicant's arguments with respect to claims 1, 2, 4, 6-10 and 12-14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Mon-Thurs 6:00-3:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The Central Fax Number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

March 19, 2004

Hung Vu

Hung Vu

Patent Examiner